REMARKS

Figures 1A - 1B and 2A - 2D have been objected to as not containing the legend "Prior Art." Also, Figure 1B is objected to because reference numeral 5 is used twice. Enclosed herewith is a Proposal of Drawing Correction and Transmittal of Corrected Informal Drawings. It is proposed that the legend "Prior Art" be added to Figures 1A - 1B and 2A - 2D. Also, in Figure 1B, it is proposed to change one of the occurrences of reference numeral 5 to reference numeral 3. This change would correct a clerical error. It is believed that the objections to the drawings would be overcome by the proposed drawing changes. Accordingly, acceptance of the drawing changes and the new informal drawings is respectfully requested.

Claim 1 is rejected under 35 U.S.C. §112, as being indefinite. The claim has been amended to address the Examiner's objection such that it is believed that the rejection is overcome. Accordingly, reconsideration of the rejection of Claim 1 under 35 U.S.C. §112, is respectfully requested.

Claims 1-9 are rejected under 35 U.S.C. §103(a) as being unpatentable over the applicants' admitted prior art (AAPA) in view of Nakamura, et al. (U.S. Patent No. 6,222,225). In view of the amendments to the claims and the following remarks, the rejections are respectfully traversed, and reconsideration of the rejections is requested.

The applicants' invention is directed to a method of fabricating a non-volatile memory device. According to the method, a tunnel insulating layer, a conductive layer and a first insulating layer are deposited over a semiconductor substrate, and the resultant structure is selectively etched to form trenches. A second insulating layer is deposited over the structure to fill the trenches. Then, portions of the second insulating layer are selectively removed to form element isolation regions composed of the second insulating layer in the trenches. The first insulating layer is then removed. Next, chemical mechanical polishing (CMP) is performed on the structure to selectively remove the second insulating layer until the top surface of the second insulating layer is substantially even with the top surface of the conductive layer. During this process, the conductive layer is used as a CMP stopping layer.

The amended claims now more clearly set forth the features of the invention. Specifically, the claims now set forth that the CMP process is performed until the surface of the conductive layer is substantially even with the surface of the second insulating layer. It is believed that with this clarifying language added to the amended claims, the claims clearly distinguish the cited prior art.

The AAPA fails to teach selectively removing the second insulating layer by CMP using the conductive layer as a CMP etching stop layer.

The Nakamura, et al. reference teaches a method of manufacturing a semiconductor device. An element isolation insulation film 14 is formed within trenches 13. A floating gate electrode 16, consisting of a lower gate electrode 16a and an upper gate electrode 16b is formed over a substrate 11 with a tunnel insulating film 15 interposed therebetween. Referring to Figures 5E and 5F of Nakamura, et al., and the corresponding description thereof at column 5, lines 48-67, the element isolation insulation film 14 is etched by an isotropic etching method such as a wet etching method. The etching is controlled such that the rounded corner regions A of the element isolation insulation film 14, which are caused by the etching process, do not vertically extend down to the tunnel insulation film 15. As a result, following the etching process, the top surface of the element isolation insulation film 14, is positioned above the surface of the floating gate electrode 16a (see column 5, lines 62-64). Hence, the element isolation insulation film 14 in Nakamura, et al. is not etched until its surface is even with the surface of the gate electrode 16a.

Accordingly, the Nakamura, et al. reference fails to teach or suggest the invention set forth in the amended claims. Specifically, Nakamura, et al. fail to teach or suggest selectively removing a second insulation layer using a CMP process until the surface of the conductive layer is substantially even with the surface of the second insulating layer.

Since neither the APA nor the Nakamura, et al. reference teaches or suggests the invention set forth in the amended claims, their combination also fails to provide such teaching or suggestion.

As noted above, Nakamura, et al. teach removing the element isolation insulation film 14 by an isotropic etching method. The Examiner states that one of ordinary skill in the art would apply a CMP process to remove a trench filling insulator. The applicants respectfully point out

that there is no suggestion in the Nakamura, et al. reference of applying CMP to the element isolation insulation film 14. Furthermore, CMP would not provide the result taught by the reference. Specifically, referring again to column 5, lines 62-64, application of a CMP process would likely result in the top surface of the element isolation insulation film 14 being level with the floating gate layer 16a. However, as is taught by the Nakamura, et al. reference, the surface position of the element isolation insulation film 14 is higher than that of the floating gate electrode 16a. This could not likely be accomplished by employing a CMP process. Accordingly, there would be no modification to apply a CMP process to the manufacturing method taught by Nakamura, et al.

Neither the AAPA nor the Nakamura, et al. reference, taken alone or in any combination, teaches or suggests the invention claimed by the applicants in the amended claims. Also, it is believed that there would be no motivation to combine the applicants' claimed CMP process to the method taught by Nakamura, et al. Accordingly, it is believed that the amended claims are allowable over the cited prior art, and reconsideration of the rejections of the claims under 35 U.S.C. §103(a) based on the AAPA and the Nakamura, et al. reference is respectfully requested.

Attached hereto is a marked-up version of the changes made to the application by the current Amendment. The attached pages are captioned "Version with Markings to Show Changes Made."

In view of the foregoing remarks, it is believed that all claims pending in the application are in condition for allowance, and such allowance is respectfully solicited. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

Date: 9/19/02

Mills & Onello, LLP
Eleven Beacon Street, Suite 605
Boston, MA 02108
Telephone: (617) 994-4900
Facsimile: (617) 742-7774

Steven M. Mills
Registration Number 36,610
Attorney for Applicants

Version with Markings to Show Changes Made

1. (Amended) A method of fabricating a non-volatile memory device having a tunnel insulating layer, comprising:

sequentially depositing said tunnel insulating layer, a conductive layer, and a first insulating layer over a semiconductor substrate, said tunnel insulating layer including at least two portions of different thicknesses;

selectively etching the resultant structure to a given depth to form trenches;

depositing a second insulating layer over said structure including said trenches;

selectively removing said second insulating layer so as to form element isolation regions composed of the trenches filled with said second insulating layer;

removing said first insulating layer; and

selectively removing said second insulating layer using a chemical mechanical polishing (CMP) process until [said] a surface of the conductive layer is [exposed] substantially even with a surface of the second insulating layer, the conductive layer being used as a stopping layer for the CMP process.

J:\SAM\0219\amendmenta.wpd